



US005682554A

United States Patent [19]
Harrell

[11] Patent Number: **5,682,554**
[45] Date of Patent: **Oct. 28, 1997**

[54] APPARATUS AND METHOD FOR
HANDLING DATA TRANSFER BETWEEN A
GENERAL PURPOSE COMPUTER AND A
COOPERATING PROCESSOR

[75] Inventor: Chandee B. Harrell, Mountain View,
Calif.

[73] Assignee: Silicon Graphics, Inc., Mountain View,
Calif.

[21] Appl. No.: 557,928

[22] Filed: Nov. 14, 1995

Related U.S. Application Data

[63] Continuation of Ser. No. 5,004, Jan. 15, 1993, abandoned.

[51] Int. Cl. ⁶ G06F 13/00

[52] U.S. Cl. 395/877; 395/250; 395/200.13

[58] Field of Search 395/250, 877,
395/200.13

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,062,059	12/1977	Suzuki et al.	395/250
4,208,713	6/1980	Berg	395/185.06
4,455,608	6/1984	Suzuki et al.	395/250
4,761,800	8/1988	Lese et al.	375/370
4,847,812	7/1989	Lodhi	365/221
4,860,193	8/1989	Bentley et al.	395/250
4,888,739	12/1989	Frederick et al.	365/221
5,003,463	3/1991	Coyle et al.	395/877
5,237,660	8/1993	Weber et al.	395/250
5,241,660	8/1993	Michael et al.	395/250
5,249,271	9/1993	Hopkinson et al.	395/377
5,261,076	11/1993	Shamshirian	395/500
5,377,184	12/1994	Beal et al.	370/231
5,390,299	2/1995	Rege et al.	395/250
5,473,756	12/1995	Traylor	395/250

Primary Examiner—William M. Treat

Assistant Examiner—Kenneth R. Coulter

Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

An apparatus in a computer system for handling data transfer between a first data processing system and a second data processing system is described. The apparatus includes a buffer for storing data received from the first system at a first data transfer rate and then transferred to the second system at a second data transfer rate. The buffer generates a first indication signal when substantially full and a second indication signal when substantially empty. A first counter counts a first predetermined time interval when receiving the first indication signal, and generates a third indication signal when reaching the first predetermined time interval. The first counter stops counting and returns to an initial state when not receiving the first indication signal. A second counter counts a second predetermined time interval when receiving the second indication signal, and generates a fourth indication signal when reaching the second predetermined time interval. The second counter stops counting and returns to the initial state when not receiving the second indication signal. A first logic causes the first system to delay sending the data to the buffer when the first counter receives the first indication signal to count toward the first predetermined time interval, and causes the first system to stop sending the data when the first counter generates the third indication signal. A second logic causes the second system to delay receiving the data from the buffer when the second counter receives the second indication signal to count toward the second predetermined time interval, and causes the second system to stop receiving the data when the second counter generates the fourth indication signal.

4 Claims, 5 Drawing Sheets

